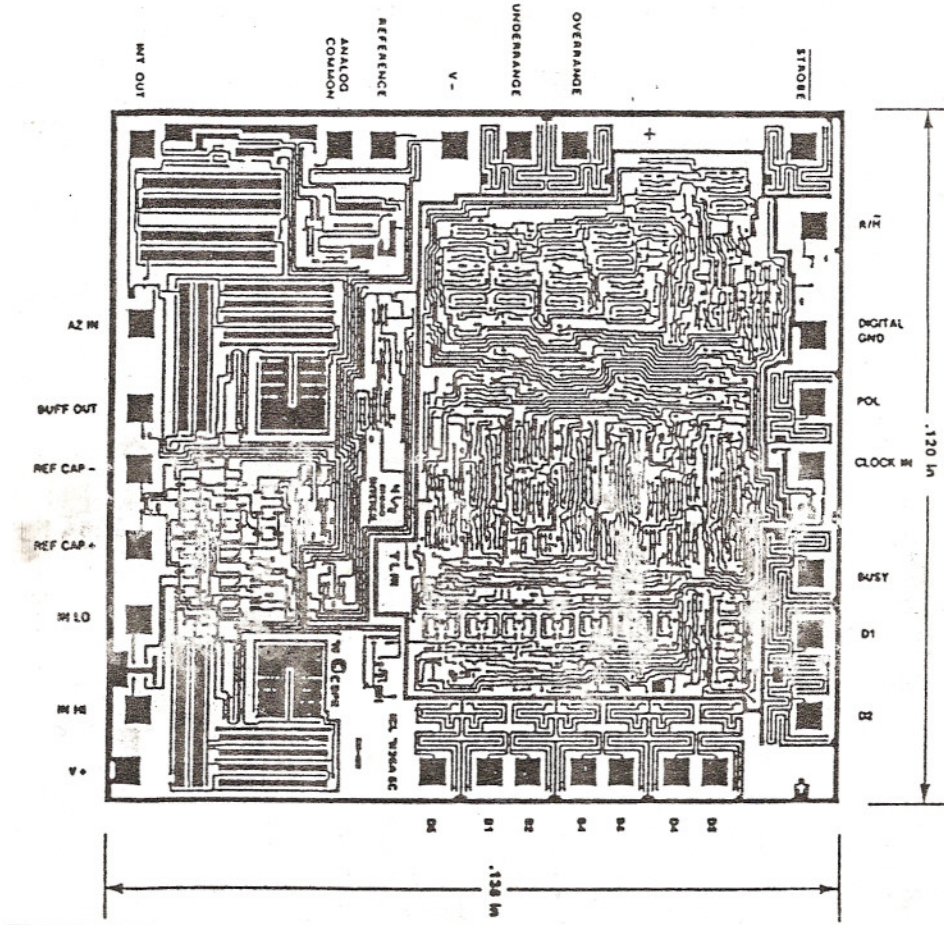




# Sierra Components, Inc.

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Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



**Topside Metal: Al**  
**Backside: Si**  
**Backside Potential:**  
**Mask Ref:**  
**Bond Pads : .004 min**

**APPROVED BY: CB**  
**MFG: Intersil**

**DIE SIZE: .120" x .138"**  
**THICKNESS: .019"**

**DATE: 2/6/01**  
**P/N: ICL7135**